Compherensive Design of a 100 kW/400 V High Performance AC-DC Converter

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Abstract. *In this paper, a comprehensive design for a 100 kW/400 V, three-phase pulse-width modulated (PWM) AC-DC converter is presented that serves as the front-end power supply for wide-range varying active load. This power supply includes two series stages; a six-switch AC-DC boost converter and a DC-DC buck converter to regulate 400 VDC at load side. The design of all inductors and capacitors is fulfilled using mathematical expressions. In addition, small signal modelling and controller design are presented in order to raise the design efficiency of the proposed converter. Also, due to the high power application, improved soft-switching techniques are applied. Furthermore, systematic approach to design an input EMI filter for DC-DC converter is explained. The simulation results performed by PSCAD software show that high performance of the proposed power supply is obtained in terms of stability, high power factor, high efficiency and low total harmonic distortion (THD).*

Keywords

AC-DC converter, controller design, small signal modelling, soft-switching technique.

1. Introduction

Three-phase AC-DC electric power conversion is widely employed in diverse applications such as adjustable-speeds drive, uninterruptible power supplies, HVDC systems, etc. [1], [2], [3]. Conventionally, AC-DC converters known as rectifiers are developed using diodes and thyristors to provide uncontrolled and controlled DC power. They have poor power quality, low power factor, high THD and low efficiency. Besides, they need large size of AC and DC filters. Nowadays, it is a common concern to use converters which provide reduced size, high power factor, high efficiency, low THD and well controlled DC voltage to present flexible system operation. Therefore, with the advent of new solid-state self-commutating devices such as IGBTs, MOSFETS, GTOs, etc., new converters are known as switch-mode rectifiers (SMRs), power factor correctors (PFCs), PWM rectifiers, multilevel and multi-pulse rectifiers [4], [5].

Appropriate modeling and control of PWM converters are increasingly being regarded in high power applications. As design of inductors and capacitors in power converters are based on the requirements of application, proper analytical expressions should be fulfilled. Also, in most cases of converters' controller design, there are two steps: selection of modulation strategy, which corresponds to open-loop control, and design of dynamic closed-loop control. Therefore, development of converters' small signal models is the best well-known approach to design proper controller [6], [7], [8].

High-power converters suffer considerably from low switching frequency due to the high switching losses. Thus, adverse control bandwidth and large passive components are achieved by low switching frequency. On the other hand, since high switching noise is more intense in high power converters, soft switching techniques are the best options to improve switching noise as well as switching frequency. In high power converters, zero-current-transition (ZCT) technique is a pleasing method, where the IGBTs are power devices [9], [10]. The topology of the presented 100 kW/400 V AC-DC converter is shown in Fig. 1. It includes two stages: a six-switch AC-DC boost converter equipped with soft switching technique in series with a soft switched DC-DC buck converter. The proposed converter is connected to a three-phase, 50 Hz utility grid with $V_{rms} = 220$ V.

This paper is organized as follows: Section 2. gives mathematical expressions to design passive components of the proposed topology which are essential to extract converters' small signal model and then to design controller. Section 3. presents theoretical expressions to design auxiliary circuits of improved soft switching techniques for both stages. Also, Section 4. includes the details of designed EMI filters for DC-DC buck converter. Simulation results are shown in Section 5. . Finally, in Section 6. the conclusion is drawn.

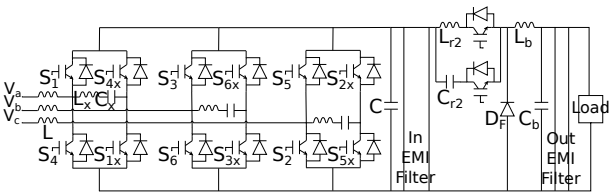


Fig. 1: The topology of proposed AC-DC converter.

2. Small Signal Modelling and Controller Design

In this section, firstly passive components of both AC-DC boost and DC-DC buck converters are designed based on the requirements of the presented application. Then, small signal models of both converters are extracted to design proper controllers.

2.1. Design of Passive Components

1) Six-Switch AC-DC Boost Converter

To obtain optimal value of boost inductor and DC-link capacitor, single-input-single-output (SISO) model of six-switch AC-DC boost converter by separating the d-axis and the q-axis dynamics is used [11]. Being non-minimum phase as an inherent feature in mentioned converter is revealed by a simple right-half-plane zero (RHPZ) in the small signal control-to-output transfer function $\vec{v}_{dc}(s)/\vec{d}(s)$. The desirable performance of converter is largely affected by RHPZ which completely depends on the boost inductor value. Since the location of the RHPZ is closest to imaginary axis in the complex s-plane under the worst operating conditions, the main aim is to design boost inductor to achieve favorable performance. On the other hand, the value of DC-link capacitor depends on the value of the boost inductor. High values of boost inductors results in low values of DC-link capacitors. Thus, there is a tradeoff between selection of boost inductor and DC-link capacitors. Figure 2 is used to gain control-to-output transfer function by SISO model. The differential equations

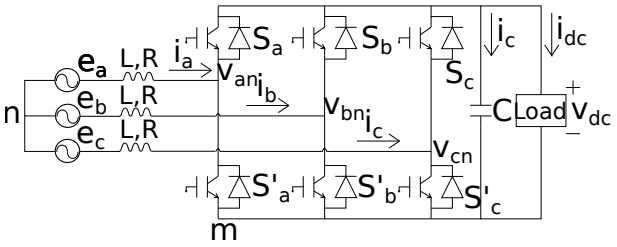


Fig. 2: A six-switch AC-DC boost converter.

of the system in the synchronous rotating d-q frame are as follows:

$$L\frac{\mathrm{d}i_d}{\mathrm{d}t} + R_L i_d - L\omega i_q = e_d - v_d, \tag{1}$$

$$L\frac{\mathrm{d}i_q}{\mathrm{d}t} + R_L i_q - L\omega i_d = e_q - v_q. \tag{2}$$

$$C\frac{\mathrm{d}v_{dc}}{\mathrm{d}t} = \frac{3}{4}(u_d i_d + u_q i_q) - i_{dc}, \tag{3}$$

where e_d and e_q are source voltages and i_d and i_d represent the input currents in $d-q$ frame. Also, the control inputs v_d and v_q are related to the d_{dc} by Eq. (4).

$$\begin{aligned} v_d &= \frac{u_d v_{dc}}{2}, \\ v_q &= \frac{u_q v_{dc}}{2}, \end{aligned} \tag{4}$$

where u_d and u_q are switching functions. Decoupling of i_d and i_d in Eq. (1) and Eq. (2) is achieved by defining v_d and v_q as Eq. (5).

$$\begin{aligned} \begin{bmatrix} v_d \\ v_q \end{bmatrix} &= \begin{bmatrix} v_{d1} + v_{d2} \\ v_{q1} + v_{q2} \end{bmatrix}. \\ \begin{bmatrix} v_{d1} \\ v_{q1} \end{bmatrix} &= \begin{bmatrix} u_{d1}\dfrac{v_{dc}}{2} \\ u_{q1}\dfrac{v_{dc}}{2} \end{bmatrix} = \begin{bmatrix} L\omega i_q \\ -L\omega i_d \end{bmatrix}. \end{aligned} \tag{5}$$

Applying decoupling control variables, differential Eq. (1), Eq. (2) and Eq. (3) are convertd to Eq. (6), Eq. (7) and Eq. (8).

$$L\frac{\mathrm{d}i_d}{\mathrm{d}t} + R_L i_d = e_d - v_{d2} = e_d - \frac{u_{d2} v_{dc}}{2}. \tag{6}$$

$$L\frac{\mathrm{d}i_q}{\mathrm{d}t} + R_L i_q = e_q - v_{q2} = -\frac{u_{q2} v_{dc}}{2}. \tag{7}$$

$$\begin{aligned} C v_{dc}\frac{\mathrm{d}v_{dc}}{\mathrm{d}t} + v_{dc} i_{dc} &= \frac{3}{2}(v_{d2} i_d + v_{q2} i_q) = \\ &= \frac{3}{4} u_{d2} v_{dc} i_d. \end{aligned} \tag{8}$$

In normal conditions, the term $v_{q2}i_q$ can be ignored, due to zero value of i_q created by control system. By substituting $u_{d2} = 1 - d = D^{'} - \vec{d}, e_d = E_d + \vec{e}_d, i_{dq} = I_{dq} + \vec{i}_{dq}, v_{dc} = V_{dc} + \vec{v}_{dc}, v_c = V_c + \vec{v}_c$ and $D^{'} = 1 - D$ in Eq. (6) and Eq. (8), small signal and dc models can be written as Eq. (9), Eq. (10), Eq. (11), Eq. (12) and Eq. (13).

$$L\frac{\mathrm{d}\vec{l}_d}{\mathrm{d}t} + R_L\vec{l}_d = \vec{e}_d - \frac{(D^{'}\vec{v}_{dc} - v_{dc}\vec{d})}{2}. \tag{9}$$

$$C\frac{\mathrm{d}\vec{v}_c}{\mathrm{d}t} + \frac{\vec{v_{dc}}}{R_{dc}} = \frac{3}{4}D^{'}\vec{l}_d - I_d\vec{d}. \tag{10}$$

$$\vec{v}_{dc} = \vec{v}_c + R_cC\frac{\mathrm{d}\vec{v}_c}{\mathrm{d}c}. \tag{11}$$

$$V_{dc} = \frac{\frac{3}{4}D^{'}E_d}{\frac{R_L}{R_{dc}} + \frac{3}{8}D^{'2}}. \tag{12}$$

$$I_d = \frac{E_d}{R_L + \frac{3}{8}R_{dc}D^{'2}}. \tag{13}$$

Therefore, small signal model of Fig. 2 in d-axis frame is shown in Fig. 3.

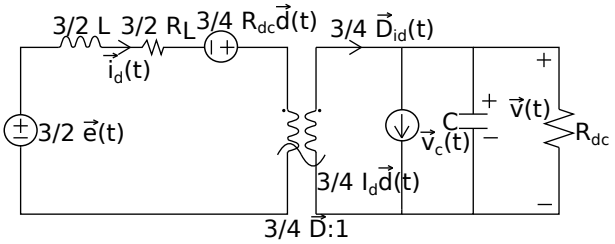


Fig. 3: Small signal model of Fig. 2 in d-axis frame.

Equation (12) and Eq. (13), express the relation between V_{dc} and I_d with steady state duty cycle D, R_L, R_{dc} and E_d. Using Eq. (12), the minimum and maximum amount of output voltage is provided by $D_{min} = 0$ and $D_{max} = 1 - \sqrt{\frac{8R_L}{3R_{dc}}}$, respectively. Therefore, the boundaries of V_{dc} can be defined by Eq. (14).

$$\left(\frac{2R_{dc}E_d}{\frac{8R_L}{3} + R_{dc}}\right) \leq V_{dc} \leq \left(\frac{\frac{3}{4}(1 - D_{max})E_d}{\frac{R_L}{R_{dc}} + \frac{3}{8}(1 - D_{max})^2}\right). \tag{14}$$

The output-to-control transfer function $\frac{\vec{v}_{dc}(s)}{\vec{d}_s}$ is calculated based on Fig. 3 as following.

$$\frac{\vec{v}_{dc}(s)}{\vec{d}(s)} = K_{DC}\frac{1 + N_1s + N_2s^2}{1 + M_1s + M_2s^2},$$

$$N_1 = \frac{(D^{'}V_{dc}R_cC - 2LI_d - 2R_LR_cI_dC)}{D^{'}V_{dc} - 2R_LI_d},$$

$$M_1 = \frac{C(8R_L(R_c + R_{dc}) + 3D^{'2}R_{dc}R_c) + 8L}{8R_L + 3D^{'2}R_{dc}},$$

$$N_2 = \frac{-2LCR_cI_d}{D^{'}V_{dc} - 2R_LI_d}, \tag{15}$$

$$M_2 = \frac{8LC(R_c + R_{dc})}{8R_L + 3D^{'2}R_{dc}},$$

$$K_{DC} = \frac{6R_{dc}E_d(3D^{'2}R_{dc} - 8R_L)}{(8R_L + 3D^{'2}R_{dc})^2}.$$

To calculate boost inductor value, suppose that the voltage drop across the inductor at full load is x % of the source voltage E_d, and then using Eq. (16) the value of L is obtained.

$$\left(\sqrt{R_L^2 + (L\omega)^2}\right)I_d = \frac{x}{100}E_d \Rightarrow$$

$$\left(\frac{(\sqrt{R_L^2 + (L\omega)^2})}{R_L + \frac{3}{8}R_{dc}D^{'2}}\right) = \frac{x}{100}, \tag{16}$$

$$L = \frac{\sqrt{\left(\frac{x}{100}\left(R_L + \frac{3}{8}R_{dc}D^{'2}\right)\right)^2 - R_L^2}}{2\pi f}.$$

In Eq. (16), to have real values for L, the term under radical must be positive. Thus, voltage drop on the boost inductor has a minimum value presented in Eq. (17).

$$x \geq \frac{100R_L}{R_L + \frac{3}{8}R_{dc}D^{'2}}. \tag{17}$$

Also, the value of $D^{'}$ in Eq. (16) can be acquired by quadratic Eq. (18) obtained from Eq. (12).

$$(R_{dc}V_{dc})D^{'2} - (2E_dR_{dc})D^{'} + \frac{8}{3}R_LV_{dc} = 0. \tag{18}$$

To solve Eq. (18), the constraint $\Delta \geq 0$ must be satisfied. Consequently, the value of boost inductor resistance has a maximum value given in Eq. (19).

$$R_L \leq \frac{3E_d^2R_{dc}}{8V_{dc}^2}. \tag{19}$$

To dictate desirable performance to the proposed converter, the capacity od DC-link capacitor is selected such that corner frequency (f_p) of complex poles in the transfer function $\frac{\vec{v}_{dc}(s)}{\vec{d}(s)}$ to be approximately three of four times less than the frequency of RHPZ. The complex poles of Eq. (15) which are as $1+\left(\frac{2\xi}{\omega_0}\right)s+\left(\frac{1}{\omega_0^2}\right)s^2=0$, have corner frequency f_p and damping factor ξ written by Eq. (20) and Eq. (21).

$$f_p=\frac{1}{2\pi}\sqrt{\frac{8R_L+3D^{'2}R_{dc}}{8LC(R_c+R_{dc})}}. \tag{20}$$

$$\xi=\frac{C(8R_L(R_c+R_{dc})+3D^{'2}R_{dc}R_c)+8L}{2\sqrt{(8LC(R_c+R_{dc}))(8R_L+3D^{'2}R_{dc})}}. \tag{21}$$

Therefore, Eq. (22) gives the value of C.

$$C=\frac{8R_L+3D^{'2}R_{dc}}{8L(R_c+R_{dc})(2\pi f_p)^2}. \tag{22}$$

In this paper, the reference output voltage for six-switch AC-DC boost converter is considered $V_{dc}=650$ V. Therefore, for $R_{dc}=4\ \Omega$ and $E_d=311.1$ V, the maximum permissible value of boost inductor resistance is $R_L\leq 0.343\ \Omega$. Suppose that $R_L=0.1\ \Omega$, then $D_{max}=0.74$ or $D^{'}_{min}=0.26$. Also, using Eq. (18), $D^{'}$ can be found as $(2600)D^{'2}-(2488.8)D^{'}+173.33=0\Rightarrow D^{'}=0.88$.

Consequently using Eq. (17), the minimum acceptable value of x would be 8 %. Finally, considering $x=12$ %, the designed value of boost inductor by Eq. (16) is $L=350$ µH. With this inductor value, the frequency of RHPZ is 485 Hz. Considering $f_p=f_{RHPZ}/3$ and $R_C=0.1$, the selected value for C would be 860 µF.

2) DC-DC Buck Converter

Evaluating DC-DC buck converter circuit in Fig. 4 during time intervals $0<t\leq DT$ (position 1, switch on) and $DT<t\leq T$ (position 2, switch off), the maximum peak-to-peak ripple current of inductor L is as follows [12]:

$$\Delta i_{Lmax}=\frac{v_0(1-D_{min})}{f_sL}, \tag{23}$$

where T is switching period, D is duty cycle, $f_S=100$ kHz is switching frequency and $V_O=400$ V is converter output voltage.

The minimum inductance required to maintain the continuous conduction mode operation for the duty cycle with the range of $[D_{min}, D_{max}]$ is given by Eq. (24).

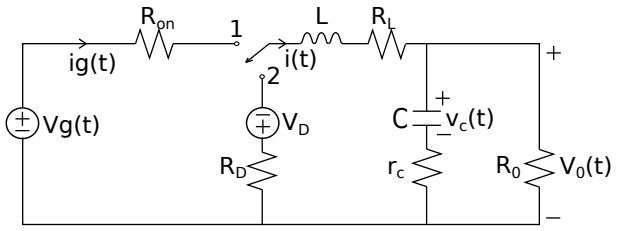


Fig. 4: Equivalent circuit of PWM DC-DC buck converter.

$$L_{min}=\frac{R_{0max}(1-D_{min})}{2f_s}, \tag{24}$$

where R_{0max} corresponds to the lowest level of converter load which is considered to be 1.5 kW. The peak-to-peak ripple voltage is independent of the voltage across C and will be determined only by the ripple voltage across the equivalent series resistance if Eq. (25) is satisfied.

$$C_{min}=\frac{\max(D_{max},1-D_{min})}{2f_sr_c}. \tag{25}$$

$$V_r=r_c\Delta i_{Lmax}. \tag{26}$$

Usually, V_r is allowed to be 1 % of output voltage. In the proposed topology, the input and output voltage of the buck converter is set to be 650 V and 400 V, respectively. Therefore, considering 100 V input voltage ripple and 90 % efficiency, minimum and maximum value of duty cycle is as: $D_{min}=\frac{V_0}{\eta V_{gmax}}=\frac{400}{0.9\cdot 750}=0.592$, $D_{max}=\frac{V_0}{\eta V_{gmin}}=\frac{400}{0.9\cdot 550}=0.807\Rightarrow \Delta i_{Lmax}=6.5$ A $\Rightarrow r_{cmax}=\frac{0.01\cdot V_0}{\Delta i_{Lmax}}=0.615$.

Suppose, r_c= 0.1 Ω, finally, the obtained minimum values for inductor and capacitor of buck converter are 217.6 µH and 40.35 µF. In this paper, selected passive components for DC-DC buck converter are 250 µH and 100 µF.

2.2. Small Signal Modelling

1) Six-Switch AC-DC Boost Converter

The first step to design a proper controller for AC-DC converters is the extraction of differential equations in the d-q frame to form converter's average model. Then, small signal analysing should be fulfilled to obtain converter's small signal model. Next, various transfer functions should be calculated using small signal model. The control method used in this paper is based on the reference [6]. Figure 5 shows standard

control scheme of the converter in d-q frame. Therefore, Eq. (27), Eq. (28) and Eq. (29) which represent the average model of a six-switch AC-DC boost converter based on line-to-line quantities are used to small signal modelling.

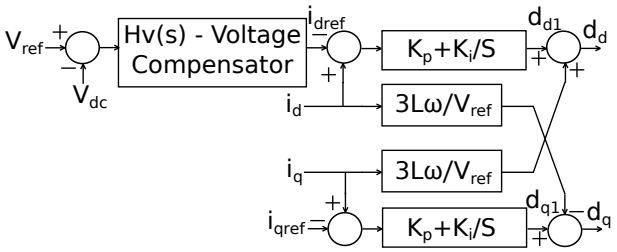


Fig. 5: Standard control scheme of six-switch boost converter in d-q frame.

$$\frac{\mathrm{d}i_d}{\mathrm{d}_t} = \omega\left(1-\frac{v_{dc}}{v_{ref}}\right)i_q - \frac{R_L}{L}i_d + \frac{1}{3L}V_d - \frac{1}{3L}d_{d1}v_{dc}. \tag{27}$$

$$\frac{\mathrm{d}i_q}{\mathrm{d}_t} = -\omega\left(1-\frac{v_{dc}}{v_{ref}}\right)i_d - \frac{R_L}{L}i_q - \frac{1}{3L}d_{q1}v_{dc}. \tag{28}$$

$$\frac{\mathrm{d}v_c}{\mathrm{d}_t} = \frac{3}{2C}\left(d_{d1}i_d + d_{q1}i_q\right) - \frac{1}{c}i_{dc}. \tag{29}$$

where i_d, i_q are line-to-line currents, d_{d1}, d_{q1} are duty cycles in d-q frame, V_d is input line-to-line voltage in d-axis and V_{ref} is desired output voltage. In these equations, cross-coupling between i_d and i_q currents is reduced by term $\left(1-\frac{v_{dc}}{V_{ref}}\right)$, when two terms $\frac{3L\omega}{V_{ref}}$ and $\frac{-3L\omega}{V_{ref}}$ are added to duty cycles d_{d1}, d_{q1}. In a similar way, by substituting $i_{dq} = I_{dq} + \vec{i}_{dq}$, $d_{d1} = D_{d1} + \vec{d}_{d1}$, $d_{q1} = D_{q1} + \vec{d}_{q1}$, $v_{dc} = V_{ref} + \vec{v}_{dc}$ and $i_{dc} = I_{dc} + \vec{i}_{dc}$ in Eq. (27), Eq. (28) and Eq. (29), small signal and dc models are written by Eq. (30), Eq. (31), Eq. (32), Eq. (33) and Eq. (34).

$$3L\frac{\mathrm{d}\vec{l}_d}{\mathrm{d}t} + 3R_L\vec{l}_d = \left(\frac{-3L\omega I_q}{V_{ref}} - D_{d1}\right)\vec{v}_{dc} - \vec{d}_{d1}V_{ref}. \tag{30}$$

$$3L\frac{\mathrm{d}\vec{l}_q}{\mathrm{d}t} + 3R_L\vec{l}_q = \left(\frac{3L\omega I_q}{V_{ref}} - D_{q1}\right)\vec{v}_{dc} - \vec{d}_{q1}V_{ref}. \tag{31}$$

$$C\frac{\mathrm{d}\vec{v}_c}{\mathrm{d}_t} = 1.5(\vec{d}_{d1}I_d + D_{d1}\vec{i}_d + \vec{d}_{q1}I_q + D_{q1}\vec{l}_q) - \frac{\vec{v}_{dc}}{R_{dc}}. \tag{32}$$

$$D_{d1} = \frac{V_d - 3R_LI_d}{V_{ref}}, D_{q1} = \frac{-3R_LI_q}{V_{ref}}. \tag{33}$$

$$I_d = \frac{v_d - \sqrt{v_d^2 - 8R_LI_{dc}V_{ref} - 36R_L^2I_q^2}}{6R_L}. \tag{34}$$

After small signal modelling, in this control method two main transfer functions $\frac{\vec{l}_q(s)}{\vec{l}_{q,ref}(s)}$ and $\frac{\vec{v}_{dc}(s)}{\vec{l}_{d,ref}(s)}$ should be acquired. According to Fig. 5, the first transfer function is used to design a PI controller for power factor correction. The designed gains for PI controller are K_P=40 and K_i=$1\cdot10^5$. The second transfer function is obtained to design voltage compensator. Equation (35) and Eq. (36) represents the main transfer functions.

Figure 6 illustrates the control diagram used to design current and voltage compensators. The control gains are determined in a way that control loops in Fig. 6 present stable performance with adequate phase and gain margins.

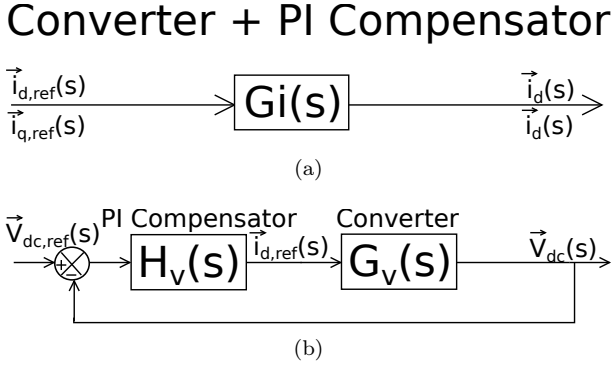


Fig. 6: Control diagram of (a) current and (b) voltage loops for a six-switch AC-DC boost converter.

In this paper, a three-pole one-zero compensator ($H_V(s)$) is used to regulate output voltage.

$$H_v(s) = K_v(s) = K_v\frac{\left(1+\frac{s}{Z_V}\right)}{s\left(1+\frac{s}{P_V}\right)\left(1+\frac{s}{P_C}\right)}. \tag{37}$$

The gain K_V should be sufficiently large to have proper phase margin. On the other hand, to have fast transient response, Z_V is determined based on Eq. (38).

$$Z_v \leq \frac{1}{4}Z_{RHP}. \tag{38}$$

Also, pole P_V is relatively placed close to Z_{RHP} after the crossover frequency, which leads to proper damping and gain margin in control system. In addition,

$$\frac{\vec{l}_q(s)}{\vec{l}_{q,ref}(s)} = \frac{\vec{l}_d(s)}{\vec{l}_{d,ref}(s)} = \frac{1+\frac{K_P}{K_i}s}{1+\frac{3R_L+K_pV_{ref}}{K_iV_{ref}}s+\frac{3L}{K_iV_{ref}}s^2}. \tag{35}$$

$$G_v(s) = \frac{\vec{v}_{dc}(s)}{\vec{l}_{d,ref}(s)} = \frac{1.5(R_{dc}K_iH+(R_{dc}X+R_pCK_iH)s+(R_pCX-3R_{dc}K_pL)s^2-(3R_pCK_pL)s^3)}{K_iV_{ref}+(K_iV_{ref}R_tC+Q)s+(3L+QR_tC)s^2+(3LCR_t)s^3}, \tag{36}$$

$$H = D_{d1}V_{ref}-3R_L, X = K_pH-3K_iL, Q = 3R_L+K_pV_{ref}, R_t = R_c+R_{dc}, R_p = R_cR_{dc}.$$

pole P_C is close to frequency $\frac{1}{R_c \cdot C}$ to compensate the effect of capacitor equivalent series resistance. All control gains of designed controller for three different levels of output power are depicted in Tab. 1.

Tab. 1: Control gains of H_V (s).

Output power	Control gains			
	K_v	Z_v	P_v	P_c
1.5 kW	137	169.5	3030.3	11628
50 kW	100	3125	7142.8	11628
100 kW	300	3125	7142.8	11628

2) DC-DC Buck Converter

A typical way to generate small signal model of DC-DC converters is the state-space description, which writes the differential equations that describe the converter [8]. Generally, the state equations of a system can be written in the compact matrix form of Eq. (39).

$$K\frac{\mathrm{d}x(t)}{\mathrm{d}t} = A\vec{x}(t)+B\vec{u}(t),$$
$$\vec{y}(t) = C\vec{x}(t)+E\vec{u}(t). \tag{39}$$

Considering Fig. 4 as our system, $\vec{x}(t)$ is a vector containing $[i(t), v_c(t)]$, $\vec{u}(t)$ contains $[V_g(t), V_D]$ and $\vec{y}(t)$ includes $[i_g(t), v_O(t)]$. Equation (39) is written with index "1" when switch is on, and with index "2" when switch is off. Afterward, Eq. (40) and Eq. (41) represent small signal model of the system.

$$K\frac{\mathrm{d}\vec{x}(t)}{\mathrm{d}t} = A\vec{x}(t)+B\vec{u}(t)+((A_1-A_2)X+$$
$$+(B_1-B_2)U)\vec{d}(t), \tag{40}$$

$$\vec{y}(t) = C\vec{x}(t)+E\vec{u}(t)+((C_1-C_2)X+$$
$$+(E_1-E_2)U)\vec{d}(t), \tag{41}$$

where $A = DA_1+D'A_2, B = DB_1+D'B_2, C = DC_1+D'C_2, E = DE_1+D'E_2$. In these equations, D is steady state duty cycle and $D' = 1-D$. The value of state vector and output variables in steady state are as follows:

$$X = -A^{-1}BU,$$
$$Y = (-CA^{-1}B+E)U. \tag{42}$$

The small signal circuits of analyzed DC-DC buck converter is shown in Fig. 7.

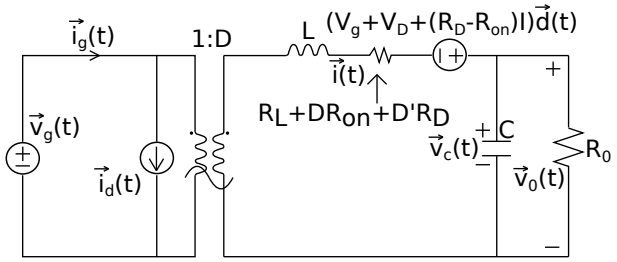


Fig. 7: Small signal model for a non-ideal DC-DC buck converter.

To control the DC-DC buck converter, the main transfer function $G_{vd}(s) = \frac{\vec{v}_O(s)}{\vec{d}(s)}$ should be calculated based on Fig. 7, while $\vec{v}_g = 0$ and $\vec{i}_{load} = 0$.

$$G_{vd}(s) = \frac{R_0 \cdot V_{it}+(V_{it}R_0CR_C)s)}{(M_0)+(M_1)s+(M_2)s^2},$$
$$V_{it} = V_g+V_d+(R_D-R_{on})I,$$
$$M_1 = L+R_0CR_C+R_{OU} \cdot R_{Ln}C,$$
$$M_2 = R_{OU} \cdot LC,$$
$$M_0 = R_0+R_{Ln},$$
$$R_{OU} = R_0+R_C,$$
$$R_{Ln} = R_L+D'R_D+DR_{on}. \tag{43}$$

Then, using control diagram of Fig. 8, compensator $G_C(s)$ is designed in a way that output voltage is regulated with wide bandwidth and zero steady state error.

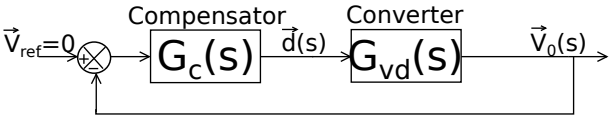


Fig. 8: Control diagram of a DC-DC buck converter.

Therefore, the best option for compensator seems to be a PID controller presented by Eq. (44).

$$G_c(s) = G_{C0}\frac{\left(1+\frac{\omega_L}{s}\right)\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)}. \tag{44}$$

For above compensator designed parameters are: $G_{C0} = 0.3$, $\omega_L = 1695$, $\omega_Z = 8333.3$, $\omega_{p1} = 117647$ and $\omega_{p2} = 3.45 \cdot 10^{11}$.

3. Soft-Switching Techniques

As in high power converters hard-switching techniques produce high switching losses and intense conductive EMI, soft-switching techniques draw more attention in this regard. It is well known that in high power converters where power switches are IGBTs, ZCT techniques are attractive. Thus, in this section two different improved ZCT (IZCT) techniques are presented for both stages of proposed topology.

3.1. IZCT Technique for Six-Switch AC-DC Boost Converter

Figure 9 shows one leg of IZCT circuit implemented for phase a. It includes two main switches (S_1 and S_2), two auxiliary switches (S_{1x} and S_{2x}) and one LC resonant tank (L_x and C_x). In this circuit, not only each phase leg has an independent soft switching, but also voltage stresses across all devices are preserved to the level of DC-link voltage [9].

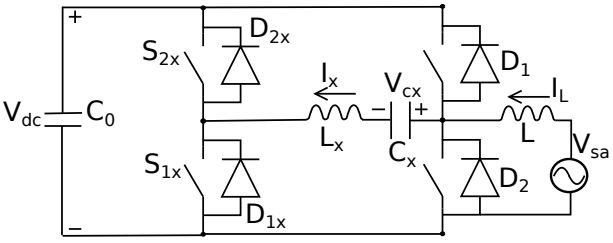


Fig. 9: IZCT circuit for phase a leg.

In Fig. 9, the relationship between main switches and corresponding auxiliary switches is diagonal. It means S_{1x} is turned on and turned off when S_1 is going to be turned on. Also, S_{1x} has another similar operation when S_1 is turned off. The gating method of both main and auxiliary switches is clearly depicted in Fig. 10.

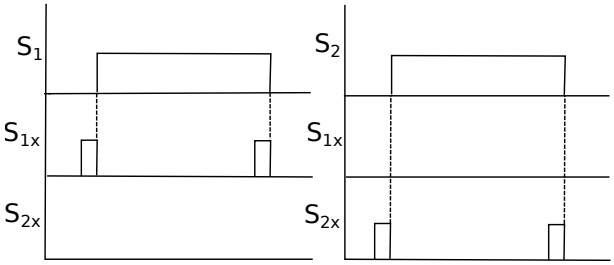


Fig. 10: Gating method in IZCT technique for six-switch AC-DC boost converter.

In order to design LC resonant tank using Eq. (45), three steps should be performed to obtain the values of T_0 and Z_0.

$$\begin{aligned} L_x &= \frac{Z_0 T_0}{2\pi}, \\ C_x &= \frac{L_x T_0}{Z_0^2}. \end{aligned} \tag{45}$$

First, normalization factors such as maximum DC-link voltage (V_{dcm}) and maximum phase current (I_{Lm}) are determined and normalized quantities are written as: $I_{Ln} = \frac{I_L}{I_{Lm}}, V_{dcn} = \frac{V_{dc}}{V_{dcm}}, Z_{0n} = Z_0\frac{I_{Lm}}{V_{dcm}}$, where I_L is phase current, V_{dc} is voltage of DC-link and Z_0 is resonant tank impedance. Second, in order to achieve soft switching operation, parameter k_{off} should satisfy Eq. (46).

$$\begin{aligned} k_{off} = \frac{3V_{dcn}}{Z_{0n}\cdot I_{Ln}} - \\ -\sqrt{4-\left(\frac{V_{dcn}}{Z_{0n}\cdot I_{Ln}}\right)^2}+1 \geq 1. \end{aligned} \tag{46}$$

The value of Z_0 and k_{off} is determined by Eq. (46). In the third step, parameter T_0 is determined by Eq. (47).

$$T_0 = \frac{\pi T_{off}}{\cos^{-1}\left(\frac{1}{k_{off}}\right)}. \tag{47}$$

where T_{off} is device dependent and it should be more than main IGBT current fall time (i.e. 0.8 µs). Afterward, the pulse width of auxiliary switches in on/off operation can be set by Eq. (48), where k_{off} is equal to k_{off} when V_{dcn}=1 and I_{Ln}=1.

$$PW_{sx} = \frac{T_0}{2}\left(1+\frac{k_{off}}{2k_{offm}}I_{Ln}\right). \tag{48}$$

In this paper, the value of maximum DC-link voltage and line current are $V_{dcm} = 650$ V and $I_{Lm} = 240$ A. Then, by designing resonant tank in this load level, we can write $I_{ln} = 1$, $V_{dcn} = 1$, $Z_{0n} = \frac{Z_0}{2.7}$. On the other hand, from Eq. (46) the maximum value of Z_{0n} is 0.833. Suppose $Z_{0n} = 0.6$, thus, other parameters can be found as following: $Z_0 = 2.7 \cdot Z_{0n} = 1.62\ \Omega \Rightarrow k_{off} = 1.52 \Rightarrow T_0 = 2.95\ \mu s \Rightarrow L_x = 0.76\ \mu H \Rightarrow C_x = 0.29\ \mu F, PW_{Sx} = 2.2\ \mu s$.

3.2. IZCT Technique for DC-DC Buck Converter

The scheme of IZCT for a DC-DC buck converter is shown in Fig. 11. This method includes an active snubber cell that is specifically suitable for IGBT-based PWM converters at high power and high frequency levels [10].

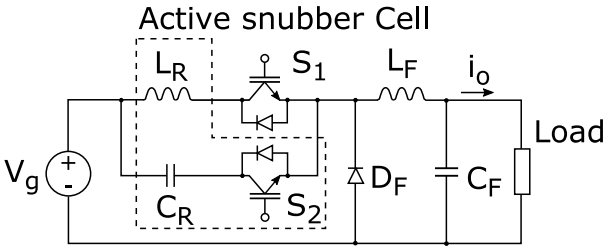


Fig. 11: DC-DC buck converter with IZCT technique.

The converter with active snubber cell can successfully operate under different load levels. To design a suitable resonant tank (L_r and C_r), the following steps for maximum load current are considered. First, resonant inductor and capacitor are chosen to let the resonant current peak (I_{RM}) be twice the maximum load current; therefore, Eq. (49) should be satisfied.

$$I_{RM} = V_g \sqrt{\frac{C_r}{L_r}} = 2I_{Omax}. \tag{49}$$

In the second step, L_r and C_r are selected such that the one half resonant cycle t_R to be equal to twice the fall time of the main IGBT. Thus, Eq. (50) is met.

$$\frac{t_R}{2} = \pi\sqrt{L_r C_r} = 2t_{f,S1}. \tag{50}$$

After designing resonant tank of active snubber cell, auxiliary switch is gated by a signal with the width equal to inverse of main switch pulse. But, according to Fig. 12, it should be delayed by T_D.

Mathematical analysis of the converter circuit demonstrated in Fig. 11, shows that the value of T_D is about a quarter resonant cycle.

$$T_D = \frac{t_R}{4} = \frac{\pi}{2}\sqrt{L_r C_r}. \tag{51}$$

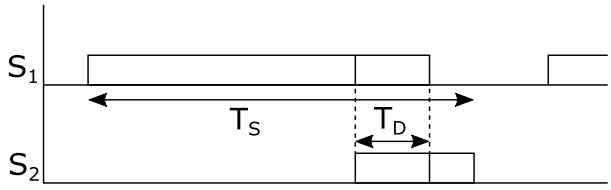


Fig. 12: Gating method in IZCT technique for DC-DC buck converter.

As in this paper the maximum value of output power is 100 kW, consequently the value of I_{Omax} is equal to 250 A. Therefore, using Eq. (49) we can write $V_g\sqrt{\frac{C_r}{L_r}} = 2I_{Omax} \Rightarrow \sqrt{\frac{C_r}{L_r}} = \frac{2 \cdot 250}{650} = 0.77 \Rightarrow C_r = 0.6 \cdot L_r$. Also, the second equation to find suitable values for passive components in active snubber cell using Eq. (50) is: $\sqrt{L_r C_r} = \frac{2t_{f,S1}}{\pi} \Rightarrow L_r C_r = \left(\frac{2 \cdot 400\ \text{ns}}{\pi}\right)^2 = 6.48 \cdot 10^{-14}$. Therefore, the value of resonant tank inductor and capacitor and the time delay required for control of auxiliary switch are: $L_r = 330$ nH, $C_r = 200$ nF, $T_D = 0.4\ \mu s$.

4. EMI Filters for DC-DC Buck Converters

It is always essential to provide EMI filters at the input and output of switching converters. Input EMI filters not only attenuate the switching noises but also protect converter and its load from input voltage disturbances [8]. Also, output EMI filters are provided to attenuate high-frequency DC voltage ripples at load side.

4.1. Input EMI Filter Design

By attenuating high-frequency input currents, input EMI filter in a DC-DC converter can limit the variation of input impedance; consequently, it can provide us with the opportunity to connect a DC-DC buck converter at load side of an AC-DC converter. Due to the wide variation of DC-DC converters' input impedance, without input EMI filters an instability in the control system can occur by the connection of DC-DC converters in series with AC-DC one. Although by adding EMI filters the former problem can be solved, a new problem appears; the input filters change the dynamic of the converters and it leads to instability of the control system again [8]. Considering Fig. 13 when input filter is added, the new transfer function of converter (G_{vd}(s)) is calculated by Eq. (52) and Eq. (53).

$$G_{vd}(s) = (G_{vd}(s)|_{z0}(s) = 0) \cdot \text{correction factor}, \tag{52}$$

$$\text{correction factor} = \frac{\left(1+\frac{Z_O(s)}{Z_N()s}\right)}{\left(1+\frac{Z_O(s)}{Z_D(s)}\right)}. \quad (53)$$

The term $G_{vd}(s)|_{zO}(s) = 0$ is the original control-

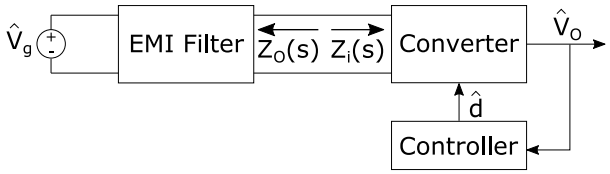


Fig. 13: Adding an input EMI filter to a converter.

to-output transfer function, $Z_O(s)$ is the output impedance of the filter, $Z_N(s)$ is the converter input impedance $Z_i(s)$ under normal operation of feedback controller which means $\vec{v}_O(s)$=0, and $Z_D(s)$ is equal to $Z_i(s)$ when $\vec{d}(s)$=0. Therefore, input EMI filter is designed in a way that the value of correction factor to be approximately unity. To reach this aim, two following inequalities should be satisfied.

$$\|Z_O(s)\| \ll \|Z_d(s)\|, \|Z_O(s)\| \ll \|Z_N(s)\|. \quad (54)$$

The topology of the used filter in this paper is presented in Fig. 14. The standard values of R_f and C_b are 1 Ω and 4700 μF. These values completely satisfy above constraints.

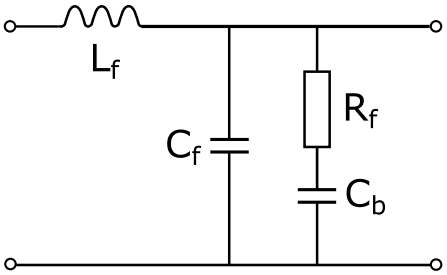


Fig. 14: The topology of input EMI filter.

For proposed topology, the inequalities Eq. (54) can be rewritten as general form of Eq. (55). On the other hand, since Z_O has the highest value in its corner frequency and Z_i has the least value in the corner frequency of Z_D, the constraint Eq. (55) may be insufficient; therefore, to have the correction factors close to unity, constraint Eq. (56) should be also met.

$$\sqrt{\frac{L_f}{C_f}} \ll \|Z_i\|_{min}. \quad (55)$$

$$\frac{1}{\sqrt{L_f C_f}} \leq \frac{\omega_0}{4}. \quad (56)$$

The bode diagram of input impedances of designed DC-DC buck converter is drawn in Fig. 15. The minimum value for Z_i is 2.8 Ω or 8.91 dB at ω_0=5320 rad·s^{-1}. Therefore using inequality Eq. (55), we can write $L_f < 7.84 \cdot C_f$. In addition, from inequality Eq. (56) following expression can be concluded. $L_f C_f \geq 14300 \cdot 10^{-12}$. Therefore, to design input EMI filter different values can be considered to satisfy above constraints. In this paper, C_f=470 μF and L_f=330 μH are selected.

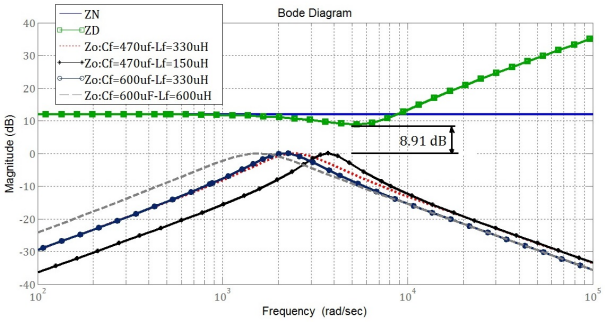


Fig. 15: Bode diagram of Z_i and different input EMI filters.

4.2. Output EMI Filter Design

In order to reduce high-frequency voltage ripples in output side, the use of one-stage low-pass LC filters of Fig. 16 is recommended [13]. The corner frequency of this filter should be significantly lower than the converter switching frequency. Usually, the Eq. (57) is regarded in the design of output EMI filters.

$$f_c = (1\ \% - 10\ \%) \cdot f_s = \frac{1}{2\pi\sqrt{L_{f0}C_{f0}}}. \quad (57)$$

In this paper, the corner frequency of filter is arbitrarily set 3 % of the switching frequency. Thus, as a typical solution, the value of capacitor C_{fo} is equal to 56 μF for an available inductor 50 μH.

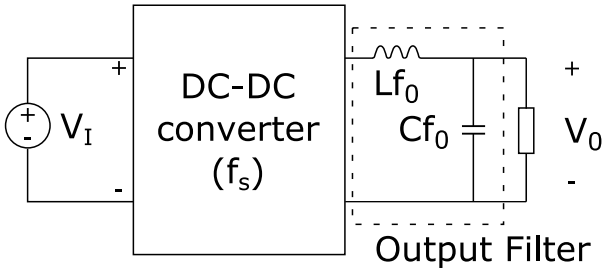


Fig. 16: The connection of a low-pass filter to a DC-DC converter.

5. Simulation

In this section, different waveforms of simulated topology of Fig. 1 in PSCAD V4.2.1, with passive components designed in previous sections are presented. To show the accuracy of the designed resonant tank for boost converter and its control, Fig. 17 is presented for phase a. For negative values of input current, switch S_1 and for positive one switch S_4 is switched under zero current. Also, voltage and current of resonant tank which show the resonance operation of designed circuit at turn on and turn off times of main switches are shown for both direction of input current.

Another characteristic of presented improved ZCT technique is to switch auxiliary switches S_{1x} and S_{4x} under zero current. Figure 18 clearly shows the current and gate signal of auxiliary switches beside corresponding input current.

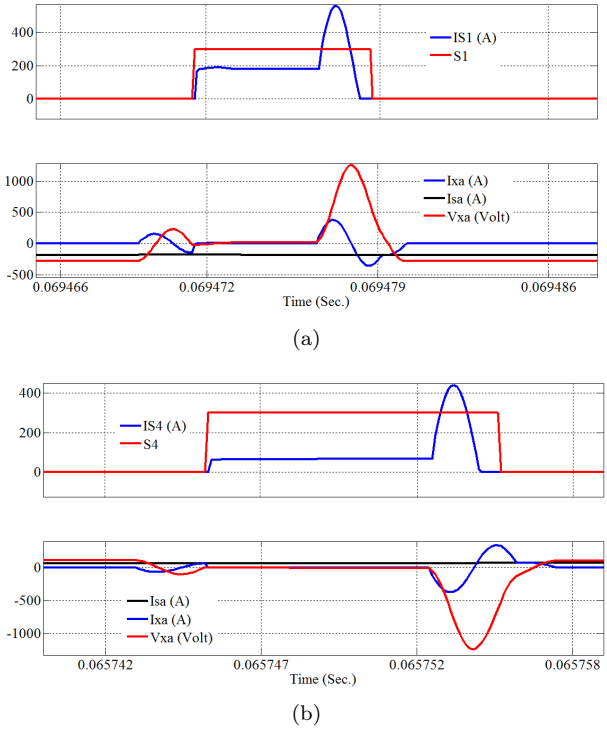


Fig. 17: Waveforms of IZCT technique in boost converter, voltage and current of resonant tank with main switches current over one switching time period, a) isa < 0, b) isa > 0.

The features of utilized IZCT technique for buck stage in the proposed converter are shown in Fig. 19. According to Fig. 19(a), switch S_1 is perfectly turned off under zero current and is turned on with near zero current. Also, S_2 is turned off under zero voltage and is turned on under near zero current. In addition, from Fig. 19(b) diode DF is turned on and off under zero voltage.

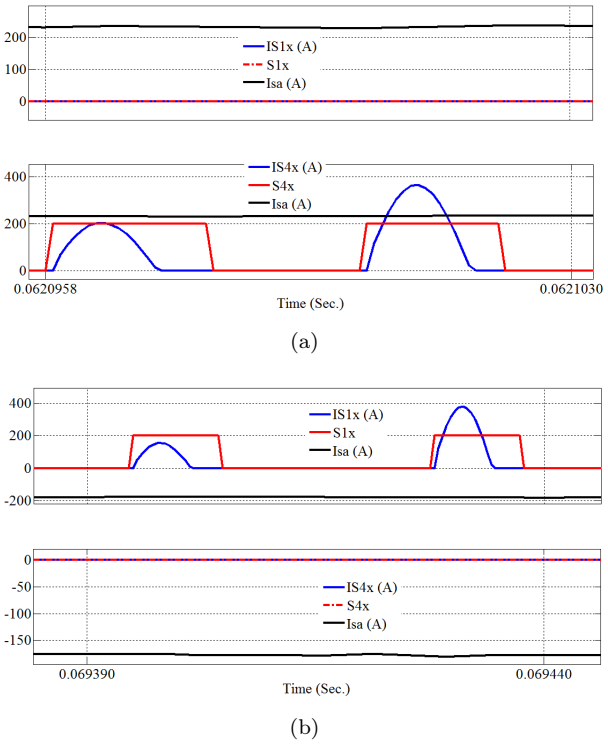


Fig. 18: Waveforms of IZCT technique in boost converter; auxiliary switches current over one switching time period, a) isa > 0, b) isa < 0.

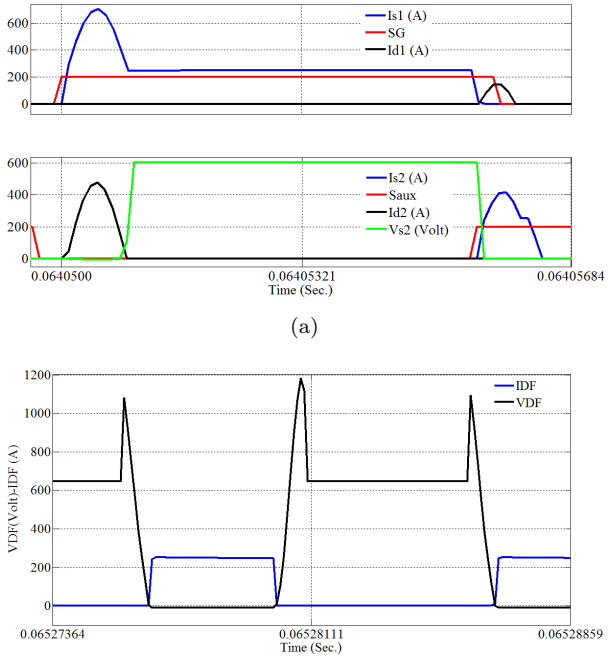
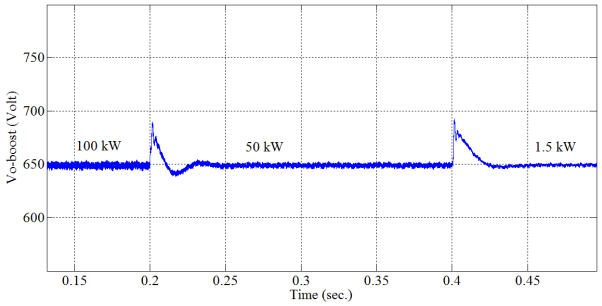
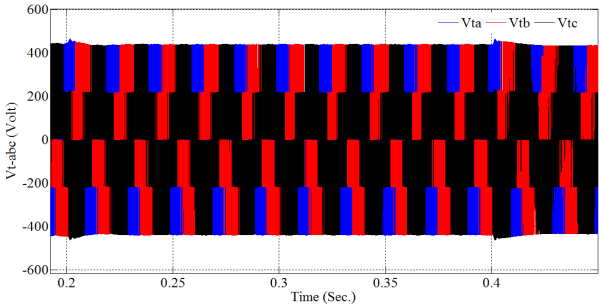


Fig. 19: Waveforms of IZCT technique in buck converter a) main and auxiliary switches' current, b) voltage and current of fast recovery diode.

It should be mentioned that in this IZCT technique the circulating energy is minimal, because one half resonance occur during operation of S_1.

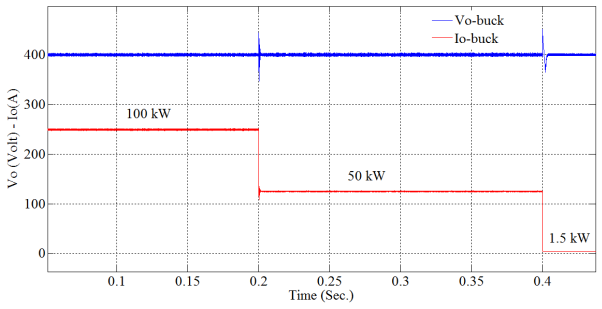


(a)

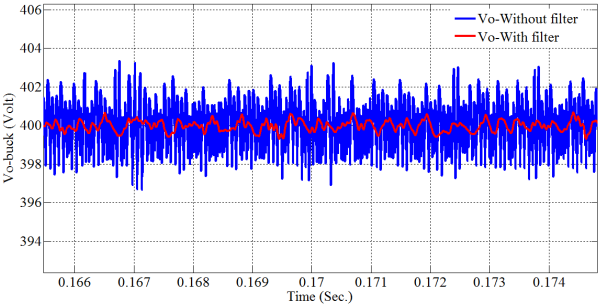


(b)

Fig. 20: a) DC-link voltage, b) boost converter terminal voltages.



(a)

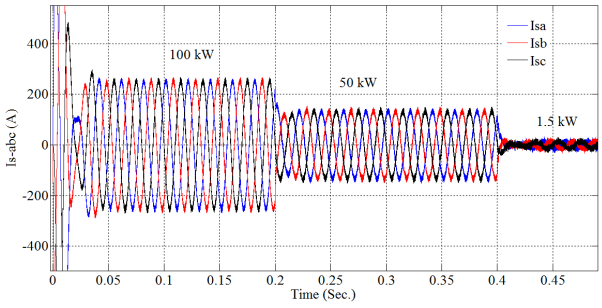


(b)

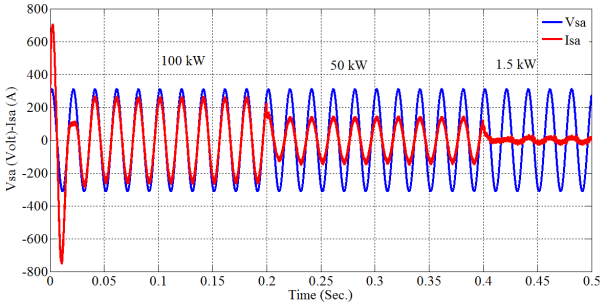
Fig. 21: a) The voltage and current at load side, b) output voltage with and without filter.

In order to show the performance of the proposed converter in terms of designed controller, Fig. 20, Fig. 21 and Fig. 22 are shown. The DC-link voltage of boost converter with the reference value of 650 V and also the terminal voltage of six-switch PWM converter are shown in Fig. 20(a) and Fig. 20(b), respectively. The output load changes from 100 kW to 50 kW at 0.2 s and then to 1.5 kW at 0.4 s. As it can be seen, fast transient response and desirable steady state error are achieved by suitable controllers which were designed in previous sections. The control strategy used in this paper to stabilize the control system of proposed converter is based on switched control strategy [14]. Several linear controllers are determined on different operating points of the converter, and an extra controller is considered to operate under a special switching law. This extra controller switches corresponding linear controller based on the specification of operating point or output load measurement.

The voltage and current at load side are shown in Fig. 21 under three different load levels. As mentioned before, the stability of control system is guaranteed by implementation of switched control strategy. But, designed buck converter does not need to this strategy. Because, by setting high gain in buck converter controller it can remain stable against load and input voltage variations. Figure 21(b) shows the effect of output EMI filter on the output voltage by attenuating high-frequency voltage ripples.



(a)



(b)

Fig. 22: a) Three-phase line currents, b) voltage and current of phase a.

Figure 22 presents network side features. The symmetrical line currents with 0.6 % THD which are received from three-phase network is shown in Fig. 22(a).

This low value of THD is obtained using Eq. (58) by having proper pattern of space vector modulation and applying it to the first stage of the proposed converter.

$$THD_I = \frac{\sqrt{I_{rms(2)}^2 + I_{rms(3)}^2 + \dots I_{rms(n)}^2}}{I_{rms(1)}}. \quad (58)$$

Also, high power factor close to unity can be found from Fig. 22(b) because boost controller forces iq to be zero in any time. It should be noted that, loss calculations prove that without any IZCT technique, maximum efficiency is approximately 91.5 %, while using IZCT techniques for both converter stages, it increases to 97.5 %.

6. Conclusion

In this paper, comprehensive planning process of a PWM AC-DC converter which supplies 100 kW load under 400 VDC is presented. The proposed converter which is supplied with a 381 Vrms three-phase network has two stages, a six switch AC-DC boost converter and a DC-DC buck converter. To have favourable performance of proposed converter, suitable controllers should be designed through exact small-signal modelling of both stages. Also, to overcome high switching losses and high EMI noises in this application due to the high load level, improved soft-switching techniques are appropriately designed and used. On the other hand, an input EMI filter is provided for DC-DC buck converter to attenuate high-frequency currents received from boost stage. This filter is an essential circuit which makes possible the connection of buck stage to boost one. In addition, since in most applications an extra filter is designed to damp high-frequency voltage ripples, in this paper a proper output EMI filter is determined at load side of the proposed converter. As simulation results indicate, soft switching techniques in conjunction with proper PWM techniques and power factor correction control loop ensure high-performance operation of presented converter in terms of efficiency, power factor and THD.

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